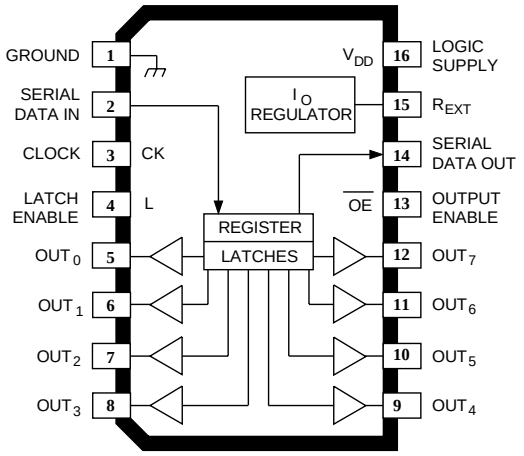
6275

PRODUCT PREVIEW

(Subject to change without notice)
December 22, 1998

8-BIT SERIAL-INPUT, CONSTANT–CURRENT LATCHED LED DRIVER

A6275ELW



Dwg. PP-029-10

Note that the A6275EA (DIP) and the A6275ELW (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... **7.0 V**
Output Voltage Range,
V_O ..... **-0.5 V to +17 V**
Output Current, I_O ..... **90 mA**
Ground Current, I_{GND} ..... **750 mA**
Input Voltage Range,
V_I ..... **-0.4 V to V_{DD} + 0.4 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6275EA and A6275ELW are specifically designed for LED-display applications. Each BiCMOS device includes an 8-bit CMOS shift register, accompanying data latches, and eight npn constant-current sink drivers. Except for package style and allowable package power dissipation, the two devices are identical.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, typical serial data-input rates are up to 20 MHz. The LED drive current is determined by the user's selection of a single resistor. A CMOS serial data output permits cascade connections in applications requiring additional drive lines. For inter-digit blanking, all output drivers can be disabled with an ENABLE input high. Similar 16-bit devices are available as the A6276EA and A6276ELW.

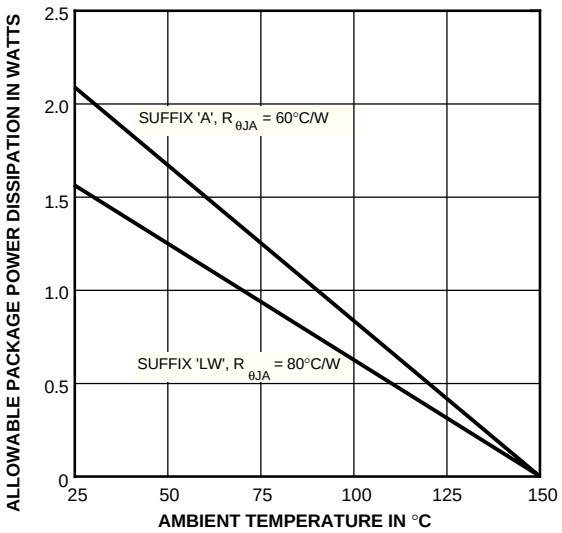
Two package styles are provided for through-hole DIP (suffix A) or surface-mount SOIC (suffix LW). Under normal applications, copper lead frames and low logic-power dissipation allow these devices to sink maximum rated current through all outputs continuously over the operating temperature range (90 mA, 0.9 V drop, +85°C).

FEATURES

- To 90 mA Constant-Current Outputs
- Under-Voltage Lockout
- Low-Power CMOS Logic and Latches
- High Data Input Rate
- Pin-Compatible with TB62705CP

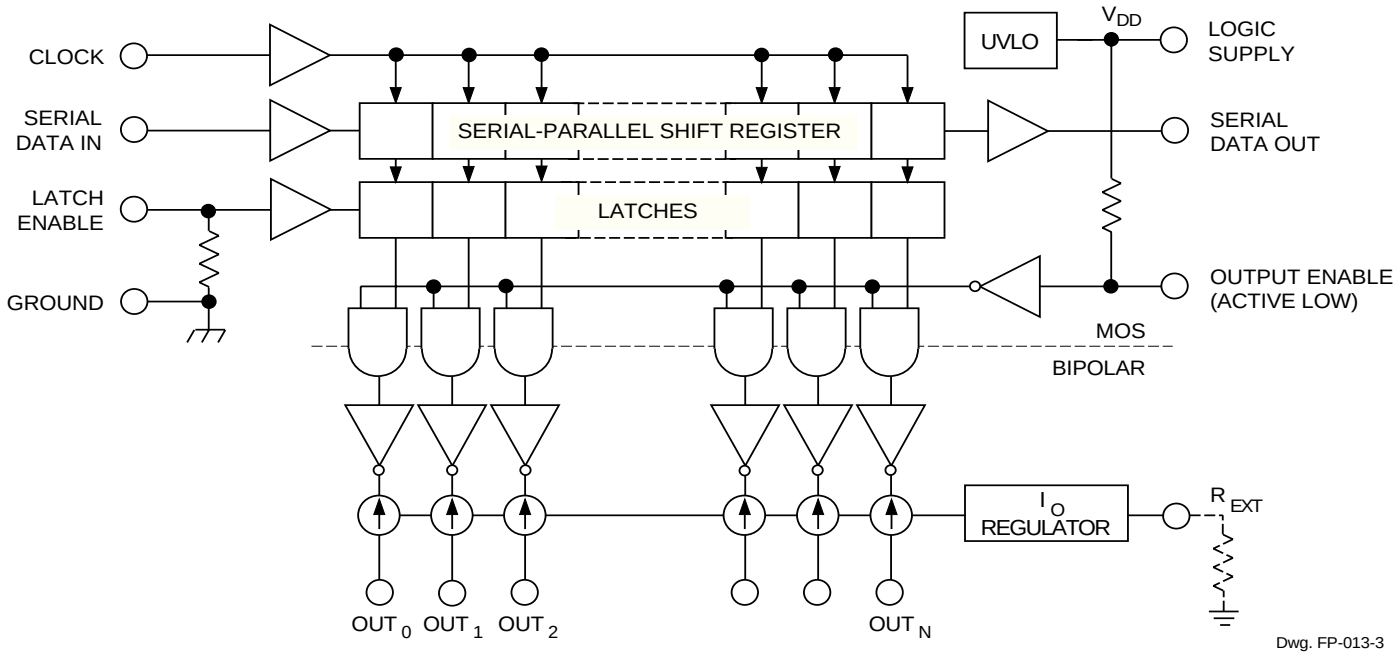
This document contains information on a product under development. Allegro MicroSystems, Inc. reserves the right to change or discontinue this product without notice.

Always order by complete part number, e.g., **A6275EA**.



Dwg. GP-018B

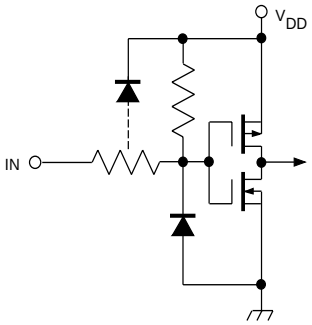
FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013-3

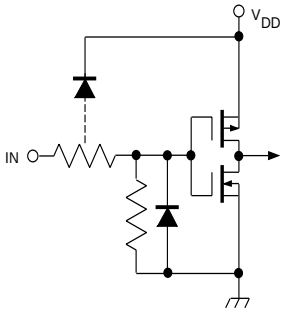
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

6275
8-BIT SERIAL-INPUT, CONSTANT-CURRENT LATCHED LED DRIVER



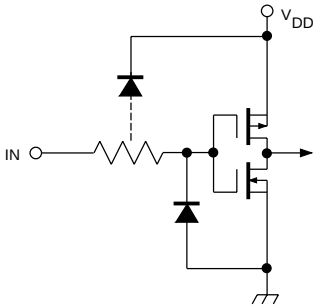
Dwg. EP-010-6

OUTPUT ENABLE (active low)



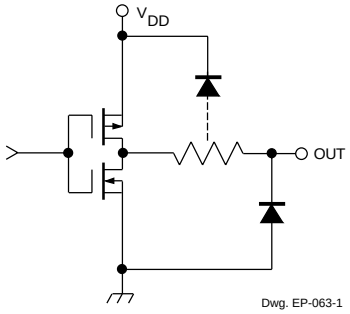
Dwg. EP-010-7

LATCH ENABLE



Dwg. EP-010-5

CLOCK and SERIAL DATA IN



Dwg. EP-063-1

SERIAL DATA OUT

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Latch Enable Input	Latch Contents	Output Enable Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐¬	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐¬	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	¬⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	H H H ... H H

L = Low Logic (Voltage) Level H = High Logic (Voltage) Level X = Irrelevant P = Present State R = Previous State

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Under-Voltage Lockout	$V_{DD(UV)}$	V_{DD} = 0 → 5 V	3.4	–	4.0	V
Output Current (any single output)	I_O	V_{CE} = 0.7 V, R_{EXT} = 250 Ω	64.2	75.5	86.8	mA
		V_{CE} = 0.7 V, R_{EXT} = 470 Ω	34.1	40.0	45.9	mA
Output Current Matching (difference between any two outputs at same V_{CE})	ΔI_O	0.4 V ≤ $V_{CE(A)}$ = $V_{CE(B)}$ ≤ 0.7 V:				
		R_{EXT} = 250 Ω	–	±1.5	±6.0	%
		R_{EXT} = 470 Ω	–	±1.5	±6.0	%
Output Leakage Current	I_{CEX}	V_{OH} = 15 V	–	1.0	5.0	µA
Logic Input Voltage	V_{IH}		0.7V_{DD}	–	V_{DD}	V
	V_{IL}		GND	–	0.3V_{DD}	V
SERIAL DATA OUT Voltage	V_{OL}	I_{OL} = 500 µA	–	–	0.4	V
	V_{OH}	I_{OH} = -1.0 mA	4.6	–	–	V
Input Resistance	R_I	ENABLE Input, Pull Up	150	300	600	kΩ
		LATCH Input, Pull Down	100	200	400	kΩ
Supply Current	$I_{DD(OFF)}$	R_{EXT} = open, V_{OE} = 5 V	–	0.8	1.4	mA
		R_{EXT} = 470 Ω, V_{OE} = 5 V	3.5	6.0	8.0	mA
		R_{EXT} = 250 Ω, V_{OE} = 5 V	6.5	11	15	mA
	$I_{DD(ON)}$	R_{EXT} = 470 Ω, V_{OE} = 0 V	5.0	10	14	mA
		R_{EXT} = 250 Ω, V_{OE} = 0 V	8.0	16	24	mA

Typical Data is at V_{DD} = 5 V and is for design information only.

SWITCHING CHARACTERISTICS at T_A = 25°C, V_{DD} = V_{IH} = 5 V, V_{CE} = 0.4 V, V_{IL} = 0 V, R_{EXT} = 470 Ω, I_O = 40 mA, V_L = 3 V, R_L = 65 Ω, C_L = 10.5 pF.

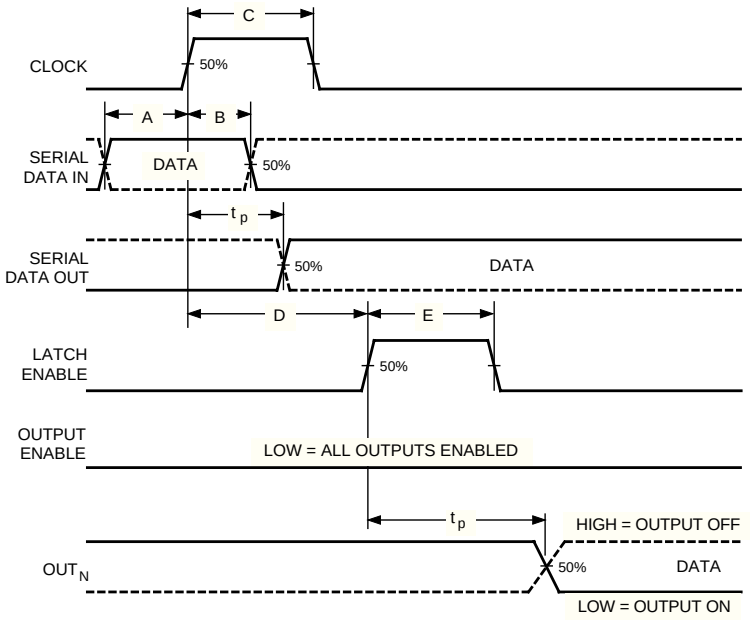
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Unit
Propagation Delay Time	t_{pLH}	CLOCK-OUT_n	-	1200	1500	ns
		LATCH-OUT_n		1200	1500	ns
		ENABLE-OUT_n	-	1200	1500	ns
		CLOCK-SERIAL DATA OUT	-	30	70	ns
Propagation Delay Time	t_{pHL}	CLOCK-OUT_n	-	700	1000	ns
		LATCH-OUT_n	-	700	1000	ns
		ENABLE-OUT_n	-	700	1000	ns
		CLOCK-SERIAL DATA OUT	-	30	70	ns
Output Rise Time	t_r	10% to 90% voltage	300	600	1000	ns
Output Fall Time	t_f	90% to 10% voltage	150	300	600	ns

RECOMMENDED OPERATING CONDITIONS

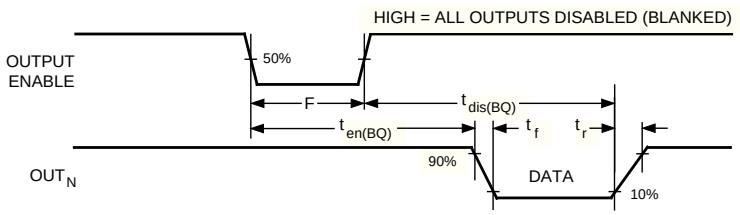
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Output Voltage	V_O		-	1.0	4.0	V
Output Current	I_O	Continuous, any one output	-	-	90	mA
	I_{OH}	SERIAL DATA OUT	-	-	-1.0	mA
	I_{OL}	SERIAL DATA OUT	-	-	1.0	mA
Logic Input Voltage	V_{IH}		$0.7V_{DD}$	-	V_{DD} + 0.3	V
	V_{IL}		-0.3	-	$0.3V_{DD}$	V
Clock Frequency	f_{CK}	Cascade operation	-	-	10	MHz

TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



Dwg. WP-029-1



Dwg. WP-030-1

A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **60 ns**
B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **20 ns**
C. Clock Pulse Width, $t_{w(CK)}$ ..... **50 ns**
D. Time Between Clock Activation and Latch Enable, $t_{su(L)}$ ..... **100 ns**
E. Latch Enable Pulse Width, $t_{w(L)}$ ..... **100 ns**
F. Output Enable Pulse Width, $t_{w(OE)}$ ..... **4.5 µs**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

— Max. Clock Transition Time, t_r or t_f ..... **10 µs**

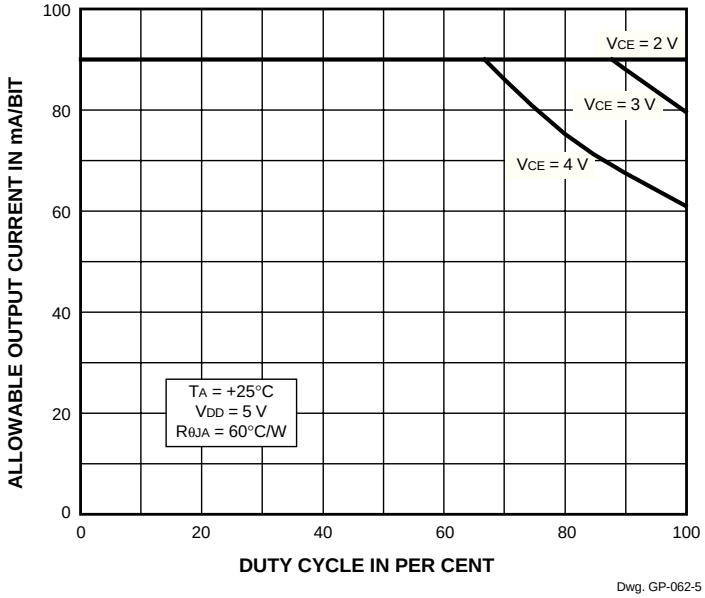
Information present at any register is transferred to the respective latch when the LATCH ENABLE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the LATCH ENABLE is held high. Applications where the latches are bypassed (LATCH ENABLE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

Allegro® MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

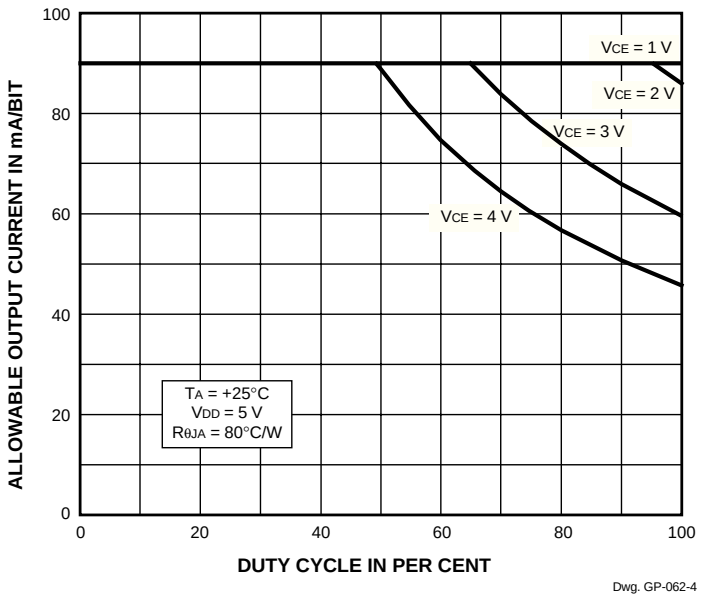
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

A6275EA

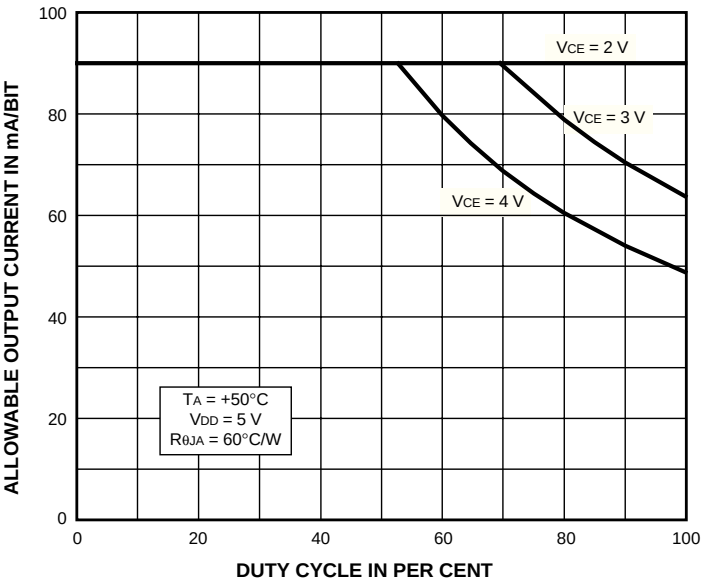


Dwg. GP-062-5

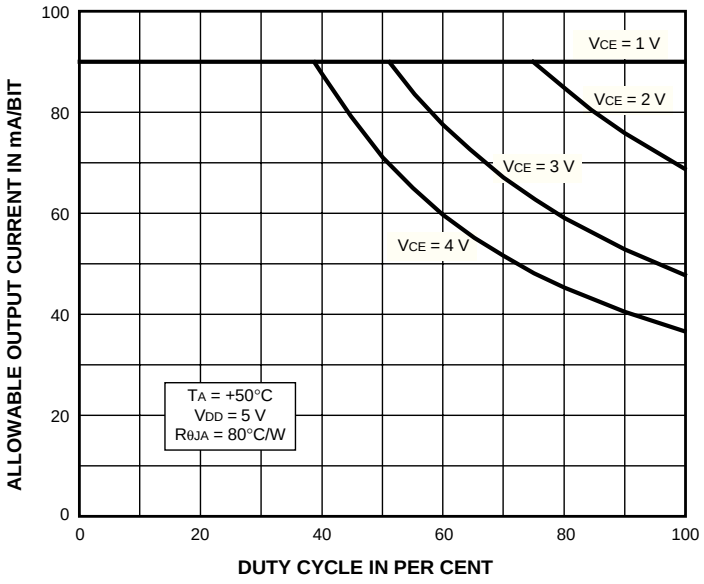
A6275ELW



Dwg. GP-062-4



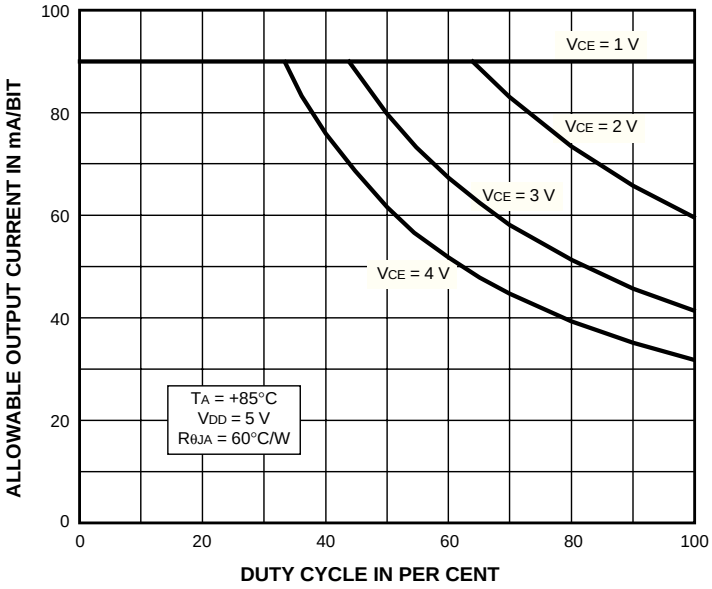
Dwg. GP-062-3



Dwg. GP-062-2

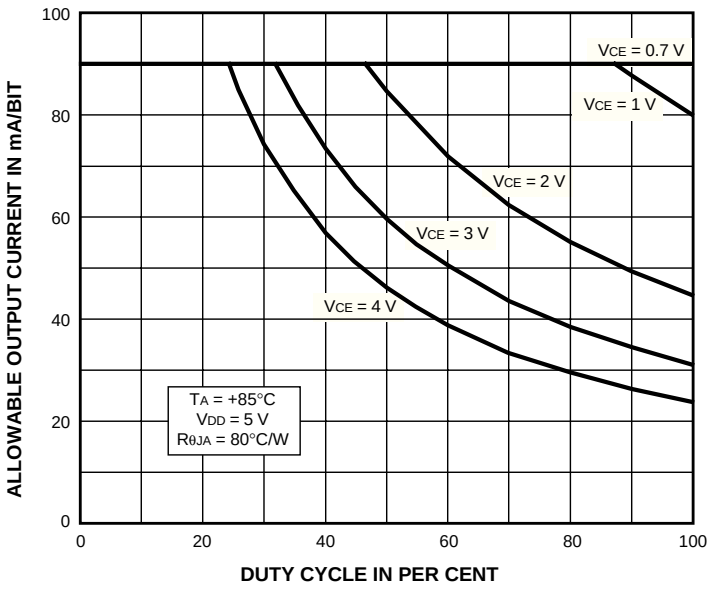
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE (cont.)

A6275EA



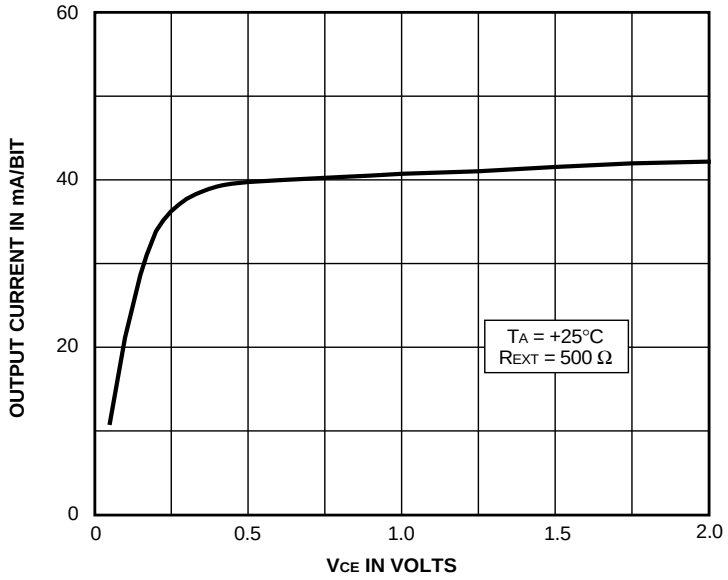
Dwg. GP-062-1

A6275ELW



Dwg. GP-062

TYPICAL CHARACTERISTICS



Dwg. GP-063

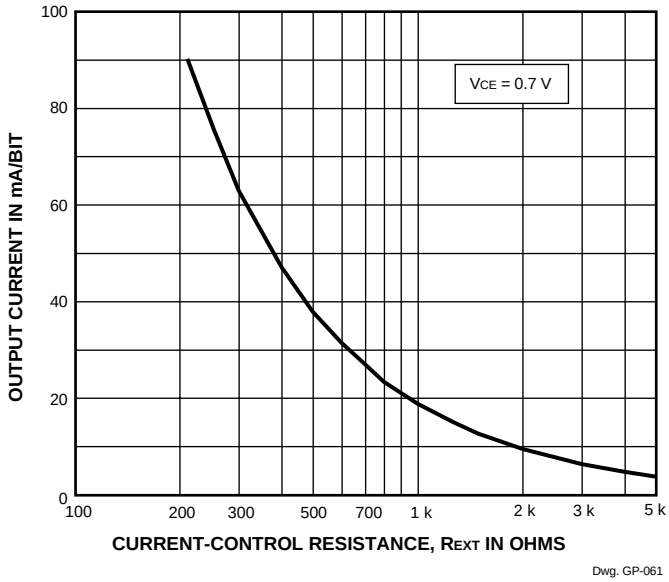
Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

TERMINAL DESCRIPTION

Terminal No.	Terminal Name	Function
1	GND	Reference terminal for control logic.
2	SERIAL DATA IN	Serial-data input to the shift-register.
3	CLOCK	Clock input terminal for data shift on rising edge.
4	LATCH ENABLE	Data strobe input terminal; serial data is latched with high-level input.
5-12	OUT_{0-7}	The eight current-sinking output terminals.
13	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
14	SERIAL DATA OUT	CMOS serial-data output to the following shift-register.
15	R_{EXT}	An external resistor at this terminal establishes the output current for all sink drivers.
16	SUPPLY	(V_{DD}) The logic supply voltage (typically 5 V).

Applications Information

The load current per bit (I_O) is set by the external resistor (R_{EXT}) as shown in the figure below.



Dwg. GP-061

Load Supply Voltage (V_{LED}). These devices are designed to operate with driver voltage drops (V_{CE}) of 0.4 V to 0.7 V with LED forward voltages (V_F) of 1.2 V to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will be increased significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage or to set any series dropping voltage (V_{DROP}) as

$$V_{DROP} = V_{LED} - V_F - V_{CE}$$

with $V_{DROP} = I_o \bullet R_{DROP}$ for a single driver, or a Zener diode (V_Z), or a series string of diodes (approximately 0.7 V per diode) for a group of drivers.

For reference, typical LED forward voltages are:

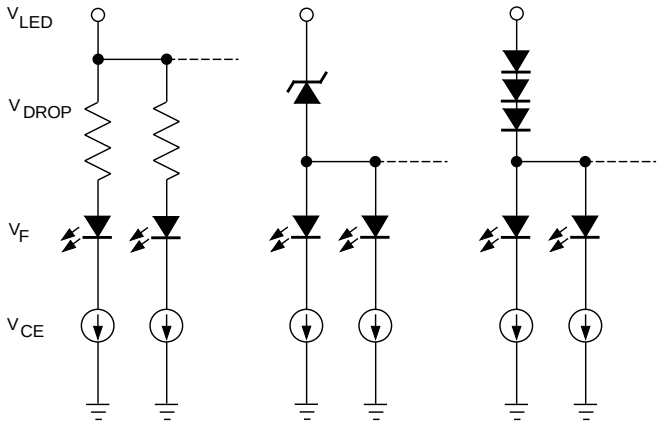
Blue	3.0 – 4.0 V
Green	1.8 – 2.2 V
Yellow	2.0 – 2.1 V
Amber	1.9 – 2.65 V
Red	1.6 – 2.25 V
Infrared	1.2 – 1.5 V

Package Power Dissipation (P_D). The maximum allowable package power dissipation is determined as $P_D max = (150 - T_A)/R_{\theta JA}$. The required package power dissipation is

$$P_D req = dc(V_{CE} \bullet I_O \bullet 8) + (V_{DD} \bullet I_{DD}).$$

When the load supply voltage is greater than 3 V to 5 V, considering the package power dissipating limits of these devices, or if $P_D req > P_D max$, an external voltage reducer (V_{DROP}) should be used.

Pattern Layout. This device has a common logic-ground and power-ground terminal. If ground pattern layout contains large common-mode resistance, and the voltage between the system ground and the LATCH ENABLE or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not operate correctly.

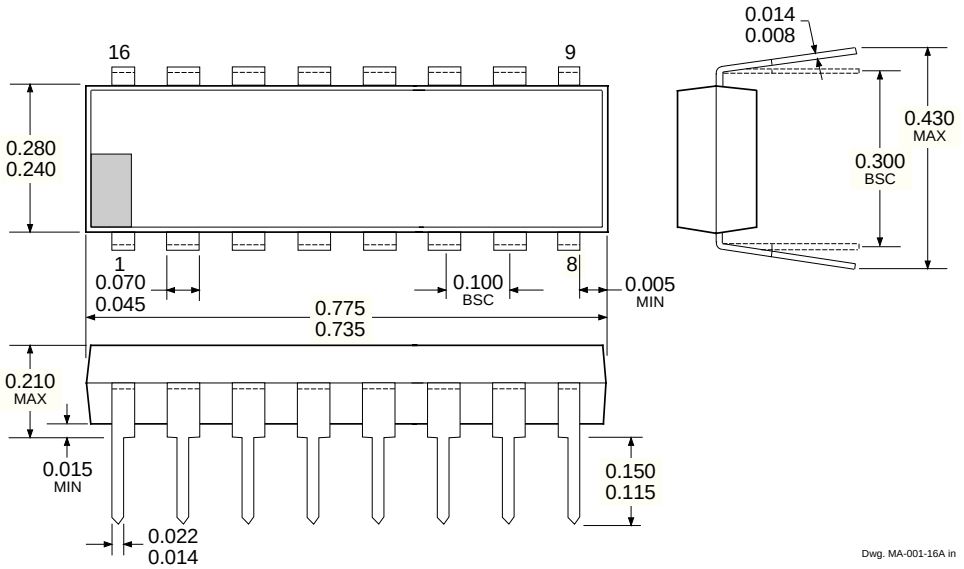


Dwg. EP-064

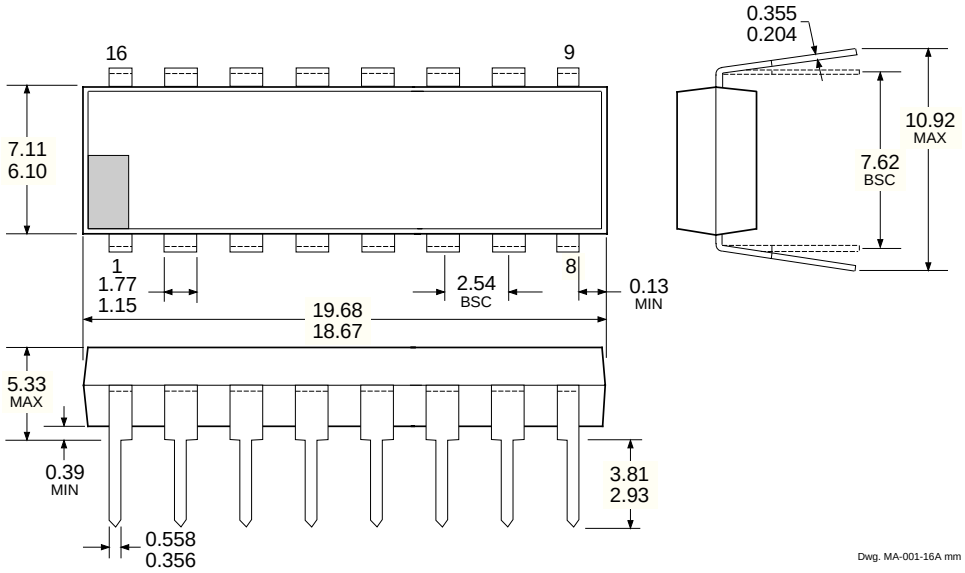
Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

A6275EA

Dimensions in Inches
(controlling dimensions)



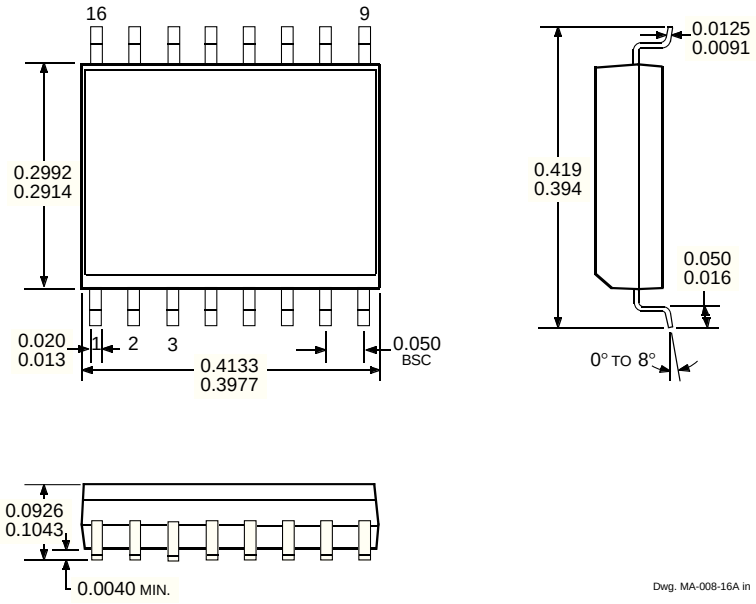
Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Lead thickness is measured at seating plane or below.

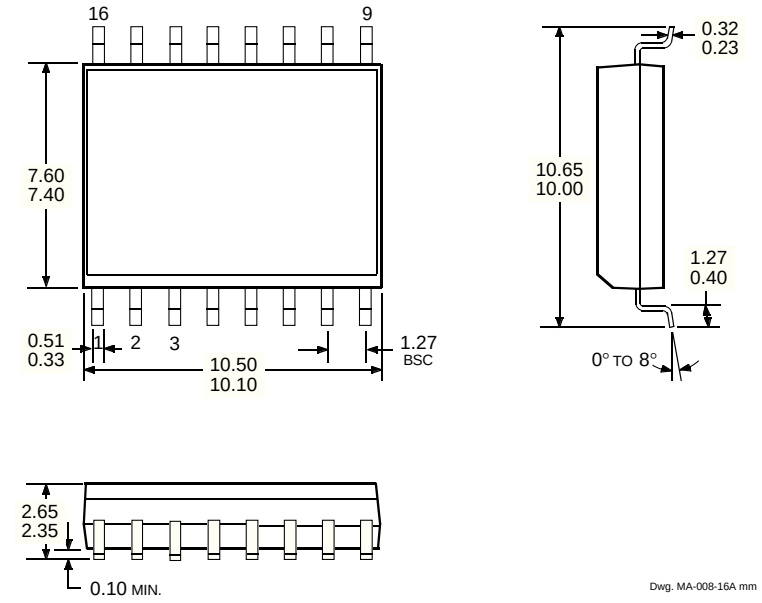
A6275ELW

Dimensions in Inches
(for reference only)



Dwg. MA-008-16A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-16A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

Allegro® MicroSystems, Inc.

115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000